A 6.75F^2/BIT VOLTAGE-CONTROL SPINTRONICS MEMORY ARRAY BY TWO MEMORY LAYERS STACKING AND BURIED-WORDLINE CELL TRANSISTORS

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I. INTRODUCTION

Voltage-Control Spintronics Memory (VoCSM) [1] is proposed as high density and low power nonvolatile memory to replace Dynamic Random Access Memory (DRAM). However, VoCSM cell contains 8 magnetic tunnel junctions (MTJs) and 9 access transistors in 1 string unit which stores 8 bits (Fig. 1). To reduce cell area, we should improve layout of cell unit. In high density 6 F^2/bit DRAM cell layout, the buried word lines and the slanted angle of active area patterns are mostly used [2]. When we adapt these high density DRAM cell techniques to the cell layout, high density VoCSM can be realized.

II. VOLTAGE-CONTROL SPINTRONICS MEMORY

The VoCSM string contains 8 MTJs and 9 access transistors. Each source node of the access transistors is connected to bitlines (BLs), and gate node of the access transistors is connected to wordline (WL). The SO layer is the bottom electrode of MTJs and connected to the selection transistor and source line (SL). To realize high density VoCSM, we should layout these elements in the small area.

III. HIGH DENSITY CELL LAYOUT

The 6 F^2 DRAM layout that contains 1 access transistor and via to storage node. The layout can be realized by using the buried word lines and the slanted angle of active area patterns. When we connect the vias to the storage node to the top electrodes of the MTJ, high density cell layout can be realized. However, there is no space to layout MTJ string and connection vias to top electrode of MTJ in same layer, we share the space to next column and stack 2 memory layers (Fig. 2). The first layer contains the access transistors of 2 strings of the VoCSM cell. The second layer contains the vias to both of the VoCSM strings and one of the VoCSM string. The third layer is the connection space to SL. The fourth layer contains the other VoCSM string. Then the 8-bit VoCSM string can be layouted above 9 access transistors which total area is 54 F^2, and the cell area is 6.75 F^2/bit.

IV. CONCLUSIONS

The 6.75 F^2/bit class VoCSM cell layout is proposed. We adapt the high density memory cell techniques and 2 memory layers stacking to the layout.

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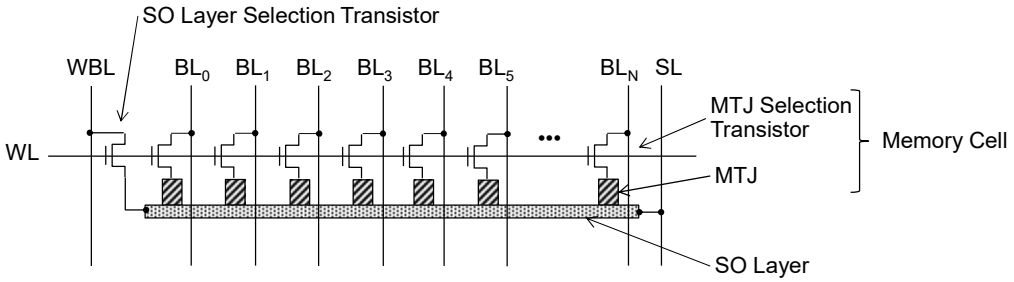

Fig. 1 A schematic drawing of the VoCSM.

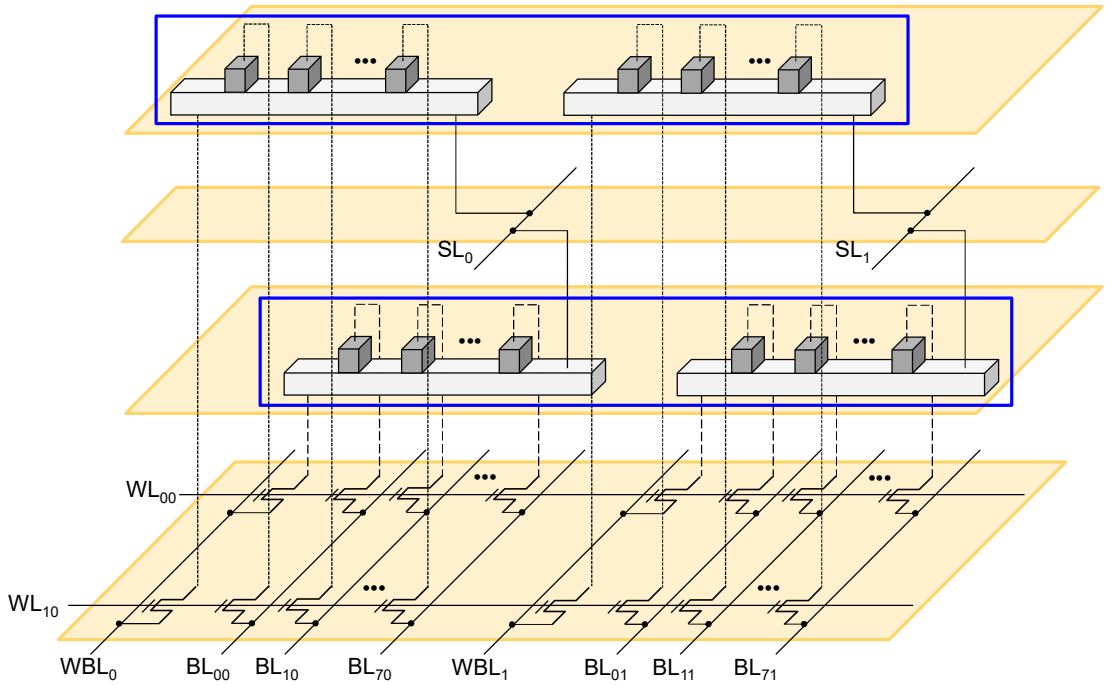

Fig. 2 Connection of access transistors and VoCSM cells.