PHYSICAL ORIGIN AND THEORETICAL LIMIT OF THE PHASE STABILITY OF A SPIN TORQUE OSCILLATOR STABILIZED BY PHASE LOCKED LOOP

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I. INTRODUCTION

The spin torque oscillator (STO) has been attracting significant interest as the next generation microwave signal source in radio frequency (RF) integrated circuits since its advent, due to its many attractive features such as ultra-small dimension, low power consumption and compatibility with semiconductor processes. To date, however, there has been no practical microwave system that actually uses an STO. One of the most serious problems hampering the adoption of STOs in real electronic systems is its poor phase stability, in other words, large phase noise. Currently, the typical phase noise levels of free running STOs are several orders of magnitude larger than those of conventional transistor based microwave oscillators. Hence, it is of paramount importance to stabilize an STO such that its signal quality meet industry specifications for the target application. For this purpose, we recently developed a phase locked loop (PL) circuit to actively stabilize an STO, and demonstrated successful phase locked oscillation characterized by an extremely sharp spectral peak [1]. Although this is a major step toward the productization of STOs, the spectrum measurement result still showed significantly larger residual phase noises than state-of-the-art semiconductor PLL chips, indicating that further performance improvement is crucial.

In this work, we performed a thorough characterization of the residual phase error of an STO stabilized by a PLL circuit, and also calculated the residual phase error using the standard linear system theory, aiming at establishing a methodology to quantitatively characterize the phase stability of the STO under free running, and clarifying the underlying physical mechanism and theoretical limit of the residual phase error of the STO stabilized by a PLL circuit.

II. EXPERIMENTAL AND ANALYSIS RESULTS

Fig. 1 shows the block diagram of the PLL circuit for stabilizing a STO built in this work. This basically follows the standard integer type PLL configuration, but with some customizations to control a STO, which has drastically different behaviors from conventional oscillators in terms of some parameters such as the bias voltage range and phase stability. The STO is nominally biased by a voltage V_{DC} to generate a microwave signal near 6.48 GHz. The generated microwave goes through the RF path of a bias-tee, amplified and downcounted by N, and eventually sent to one input of the phase frequency detector (PFD). The other input of the PFD is fed a very stable reference clock with a frequency f_r. The phase difference between these two signals is converted into a voltage signal V_E, which is filtered by a loop filter (LF) block and added to V_{DC} and fed back to the STO to dynamically tune the frequency such that the phase difference at the PDC is always minimized. Fig. 2 shows the phase error spectral density (PESD) of the STO under free running in red, phase locked to f_r = 135 MHz in purple, 270 MHz in blue and 405 MHz in green, respectively. The integration of the PESD, in other words, the area under the PESD curve, corresponds to the variance of the phase error, which is equivalent to the variance of the timing jitter. A black broken line superimposed on top of each curve is the theoretical calculation result for each oscillation condition. These results all showed excellent agreement between the experimentally observed and theoretically calculated PESD, which strongly supports the validity of the theory used in these calculations. This means that now we can assess the influence of each circuit parameter in the PLL circuit on the final performance of the STO stabilized by the PLL. The theory suggests the following. First, there

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may be some room for further reduction of the variance of the timing jitter by roughly another one order of magnitude by tightly integrating all the blocks and element in the circuit to speed up the PLL circuit response. Second, it is crucial to reduce the FESD of the free running performance of the STO in order to further reduce the residual phase error of the STO stabilized by the PLL.

In the poster, we will present the detail of these analyses such as characterization methodology, data processing algorithm and theory for calculating the PESD of the STO, as well as future direction of the STO research and development for better signal quality.

REFERENCES

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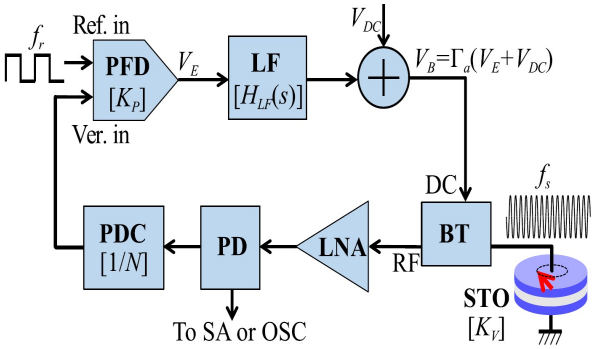

Fig. 1, Block diagram of the PLL circuit stabilizing a STO. Each functional block is labeled as, PFD: Phase Frequency Detector (proportionality constant for phase difference to voltage conversion denoted as K_P); LF: Loop Filter (transfer function denoted as $H_{LF}(s)$); STO: Spin Torque Oscillator (agility constant denoted as K_V); BT: Bias-Tee; LNA: Low Noise Amplifier; PD: Power Divider; PDC: Programmable Down Counter (divider ratio denoted as N); SA: Spectrum analyzer; and OSC: Oscilloscope. The two inputs of the PFD are abbreviated as, Ref. in: Reference frequency input; Var. in: Variable frequency input.

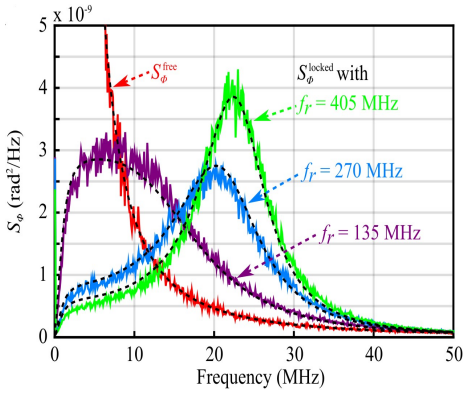

Fig. 2, PESD of the STO output signal. The four lines drawn with red, purple, blue and green represent the PESD when the STO is free running, phase locked to three different reference frequencies of f_r = 135 MHz, 270 MHz and 405 MHz, respectively. The broken line superimposed on each line is the theoretically calculated PESD.