4 GBIT DENSITY STT-MRAM USING PERPENDICULAR MAGNETIC TUNNEL JUNCTIONS WITH COMPACT BIT CELL STRUCTURE

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Spin transfer torque Magnetic Random Access Memory (STT-MRAM) has attracted considerable attention as a potential replacement for Dynamic Random Access Memory (DRAM) because of its excellent performance such as infinite endurance, fast operation, and scalability beyond 30nm feature dimension [1-4]. Furthermore, STT-MRAM enable to overcome the excessive power consumption of DRAM by taking advantage of the non-volatility of magnetic tunnel junction (MTJ) storing data "1" or "0".

Both of the mature Si-based technology and the intensive progress on MTJ allow to develop *high-density* STT-MRAM. However, the critical challenges are still manifold because MTJ fabrication is based upon an extremely tight pitch. From the array operation point of view, high performance cell transistor and MTJ are essential. Also, the distribution of parasitic resistance should be significantly improved. In this work, we demonstrate 4Gbit density STT-MRAM with optimization of integration process and MTJ fabrication [5].

Fig. 1 shows the compact bit cell structure consisting of a NMOS transistor, a pair of bit line (B/L), a circle-shape MTJ, and source line (S/L). All perpendicular MTJ using CoFeB/MgO/CoFeB and the magnetic multilayer is on top of the bottom electrode (BEC). The bottom-storage layer is used to avoid the S/L bias degeneration resulting in the degradation of write current for a parallel-to-antiparallel switching. The top electrode contact (TEC) and source line contact (SLC) are successfully patterned within 90nm-pitch. The cell projection area using 3-dimensional transistor is estimated as $9F^2$ which is very close to that of DRAM. Fig. 2 is a floorplan of 4Gbit array. The chip is divided into 8 banks, and each bank contains 512Mb array. The quarter bank corresponds to the unit array blocks consisting of the unit cell array, a sub-wordline driver (SWD) for controlling a gate bias at the cell transistor, and a local Y-switch (LYSW) for selecting a B/L or a S/L which is connected to a sense amplifier (S/A) and write driver (WD).

In order to investigate the operation window of the bit cell array, V_{dd} is modulated in the range of 1.1~1.7V and the resistance of S/A was tuned by V_{ref}. The bit cell without MTJ structure was useful to evaluate the distribution of the parasitic resistance including cell transistor, B/L, S/L, and etc. Even though the resistance of MTJ is larger than the parasitic resistance, we found that the contact process is one of key factor for a reliable read operation. Write error rate (WER) evaluation was performed for several kbits with 10^6 cycles and tunable V_{dd}. With optimized fabrication process and MTJ stacks, the average WER could be sufficiently suppressed for a reliable write operation. The magnetic distribution of the MTJ array was evaluated under the external magnetic field. The magnetic distribution strongly depends on the MTJ stack, and it was critical to ensure a low WER. We compared the bit error rate between the bit-by-bit (BbB) read-write operation and all-by-all (AbA) read-write one so as to evaluate the retention performance. It was confirmed that the error rate is identical for both chip operations. This indicates that the stored data is retained for several minutes which is the time duration for AbA write operation. 4Gbit full-functional operation was performed after replacing failure bits with redundancy cells.

4Gbit density STT-MRAM was realized with all perpendicular MTJs and compact cell structure. Both of integration technology and MTJ fabrication were optimized to demonstrate the chip operation. This achievement paves the way toward stand-alone memory application of STT-MRAM.

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REFERENCES

1) J. M. Slaughter et al., “High Density ST-MRAM Technology”, *IEDM Tech. Dig.*, 29.3.1-4, (2012).
2) C. Park, et al., “Systematic Optimization of 1 Gbit Perpendicular Magnetic Tunnel Junction Arrays for 28 nm Embedded STT- MRAM and Beyond”, *IEDM Tech. Dig*., 26.2.1-4, (2015).
3) H. Yoda et al., “High efficient spin transfer torque writing on perpendicular magnetic tunnel junctions for high density MRAMs”, *Current Appl. Phys*. vol.10, pp.e87-89 (2010).
4) T. Kishi et al., “Lower-current and fast switching of a perpendicular TMR for high speed and high density spin-transfer-torque MRAM”, IEDM Tech. Dig., 12-6, 2008.
5) S.-W. Chung et. al., “4Gbit density STT-MRAM using perpendicular MTJ realized with compact cell structure”, *IEDM Tech*. *Dig*., 27.1, (2016).
6) G. Jan et al., “Achieving Sub-ns switching of STT-MRAM for future embedded LLC applications through improvement of nucleation and propagation switching mechanisms”, Proc. of VLSI Tech. 2.4, 2016.

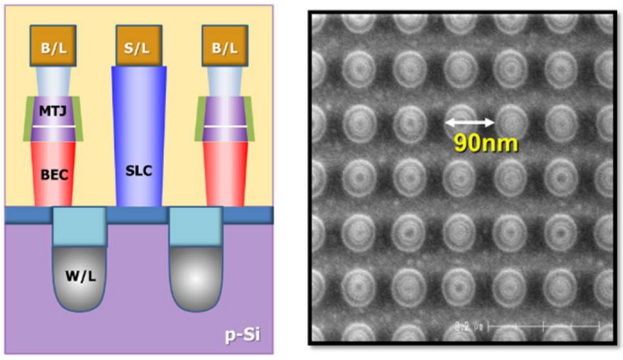

Fig. 1 (Left) Schematic diagram of bit cell and (Right) top-view SEM image after the contact patterning.

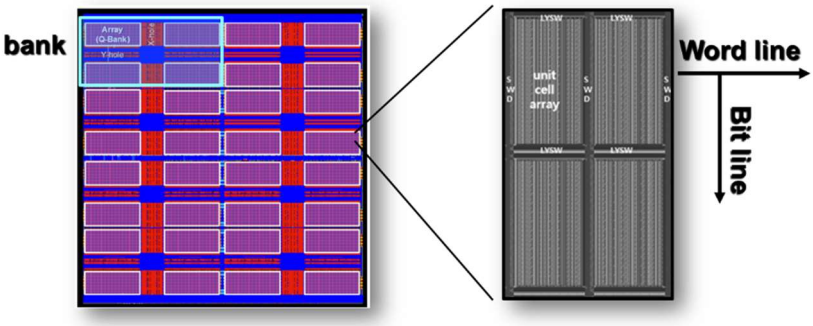

Fig. 2 (Left) 4Gbit STT-MRAM chip floor plan (Right) unit array blocks with error correction code.