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Demonstration of Nanowire Schottky Barrier Tunnel FET Opearation

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Introduction The Schottky barrier tunnel FET (SBTFET) [1] is a promising alternative for conventional MOSFET, which faces the scaling limit posed by the short channel effect. On current of SBTFET flows by tunneling through the Schottky barrier at metal source/channel interface, and the gate modulates the barrier width. SBTFET has advantages of low thermal budget, abrupt source/drain junction and no random dopant fluctuation. However, it is difficult to conduct a high density of current by tunneling, and thus it is quite important issue to secure the ON current density by employing the nanowire (NW) channel structure. In this study, we have fabricated NW-SBTFET and succeeded in demonstrating the tunneling FET operation.

Experiment The device is fabricated on lightly p-type doped (100)SOI wafer with 45nm thick Si, 145nm thick BOX and 750um Si-substrate. <110> oriented Si-NWs of 10 lines and pads are fabricated by electron beam lithography, followed by TMAH wet etching. The NWs undergo thermal oxidation in dry O_2 ambient at 850 ℃ for 3h. The width of NWs including the oxide layer are 68-120 nm. After thermal oxidation, P^+ ions are implanted at 25keV ($1.0\times10^{12}cm^{-2}$). In order to form ohmic contacts, higher dose of P^+ ($1.0\times10^{15}cm^{-2}$) is implanted into the drain side pads and annealed at 950 ℃ for 10min to activate the implanted ions. The thermal oxide is partially removed by BHF and 20nm thick Ni is deposited by ion sputtering. Then Ni silicide is formed by annealing at 410 ℃ for 120s. The unreacted Ni is removed by SPM. Finally, the oxide on the drain side pad is removed by BHF and AlSi electrodes are formed on source/drain pads. The schematic of the device structure is shown in Fig.1. Finally. FET characteristics are carried by applying backgate voltage (V_{bg}).

Results and Discussions Fig.2(a) and 2(b) show the lateral SEM image of Ni silicided NW and cross-sectional SEM image of Si-NWs. Fig.3 shows the dependence of I_d-V_{bg} characteristic on NWs width. ON current density is enhanced for V_{bg} > 20V. The enhanced current component is the tunneling current through the Schottky barrier, which was confirmed by the Fowler-Nordheim(F-N) plot[2,3]. We have performed a TCAD device simulation and confirmed that the stronger electric field concentrates on a small region around the edge of thinner NWs. Therefore, ON current density enhancement observed thinner NW device is attributed to the local electric field concentration at the NW edges.

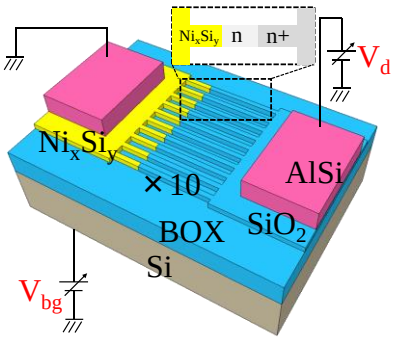

Figure 1 Schematic views of NW-SB-TFET with Ni silicide.

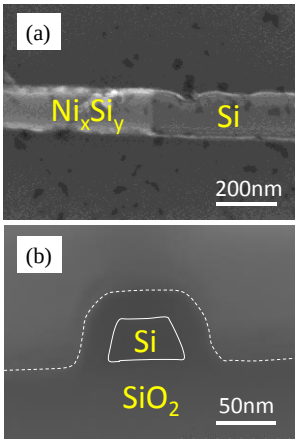

Figure 2 SEM images of NW-SB-TFET (a)lateral image and (b)cross-sectional image.

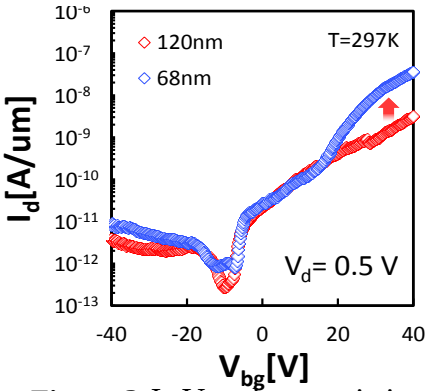

Figure 3 I_d-V_{bg} characteristics with different NW width.

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Reference

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